

DATA SHEET

SCN26562

Dual universal serial communications
controller (DUSCC)

Product specification

1995 May 01

IC19 Data Handbook

Dual universal serial communications controller (DUSCC)

SCN26562

DESCRIPTION

The Philips Semiconductors SCN26562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN26562 interfaces to synchronous bus MPUs and is capable of program-pollled, interrupt driven, block-move or DMA data transfers.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multi-function counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

This document contains the electrical specifications for the SCN26562. See SCN26562/SCN68562 User's Guide for complete functional description.

FEATURES

General Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
 - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
 - COP: BISYNC, DDCMP
 - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4Mbit/sec data rate
- Programmable bit rate for each receiver and transmitter selectable from:
 - 16 fixed rates: 50 to 38.4k baud
 - One user-defined rate derived from programmable counter/timer
 - External 1X or 16X clock
 - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
 - Single- or dual-address dual transfers
 - Half- or full-duplex operation
 - Automatic frame termination on counter/timer terminal count or DMA EOPN input
- Interrupt capabilities
 - Vector output (fixed or modified by status)
 - Programmable internal priorities
 - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
 - Bit rate generator
 - Event counter
 - Count received or transmitted characters
 - Delay generator
 - Automatic bit length measurement
- Modem controls
 - RTS, CTS, DCD, and up to four general purpose pins per channel
 - CTS and DCD programmable auto-enables for Tx and Rx
 - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbit/sec data rate Receives up to 2Mbit/sec data rate

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Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line-fill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and detection
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs line-fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	$V_{CC} = +5V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$	
	Serial Data Rate = 4Mbps Maximum	DWG #
48-Pin Plastic Dual In-Line Package (DIP)	SCN26562C4N48	SOT240-1
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCN26562C4A52	SOT238-3

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature ²	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND ³	-0.5 to +7.0	V
V_S	Voltage from any pin to ground ³	-0.5 to $V_{CC} + 0.5$	V

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 36°C/W junction to ambient for ceramic DIP, 40°C/W for plastic DIP, and 42°C/W for PLCC.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

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PIN CONFIGURATIONS

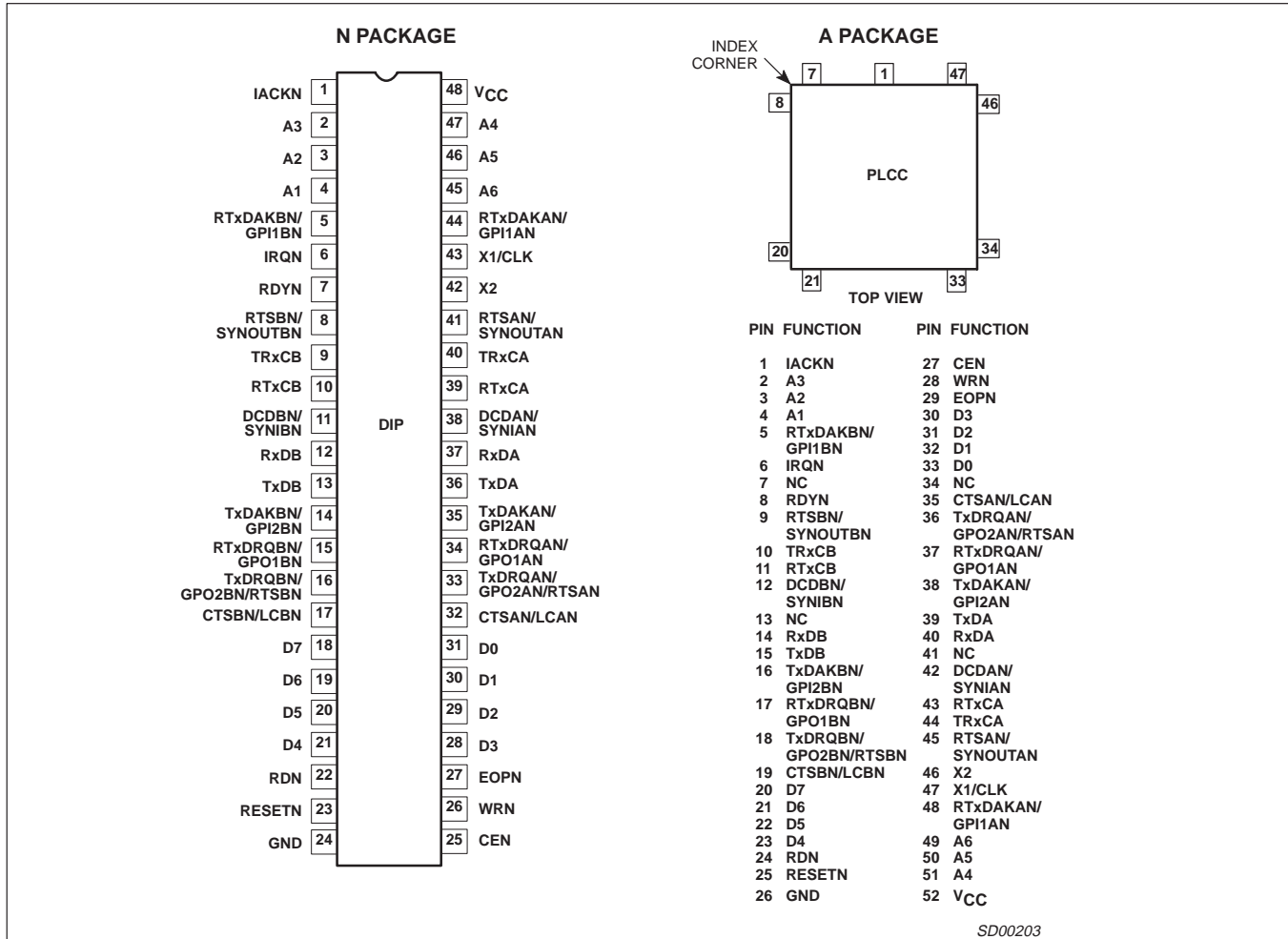


Figure 1. Pin Configurations

SD00203

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BLOCK DIAGRAM

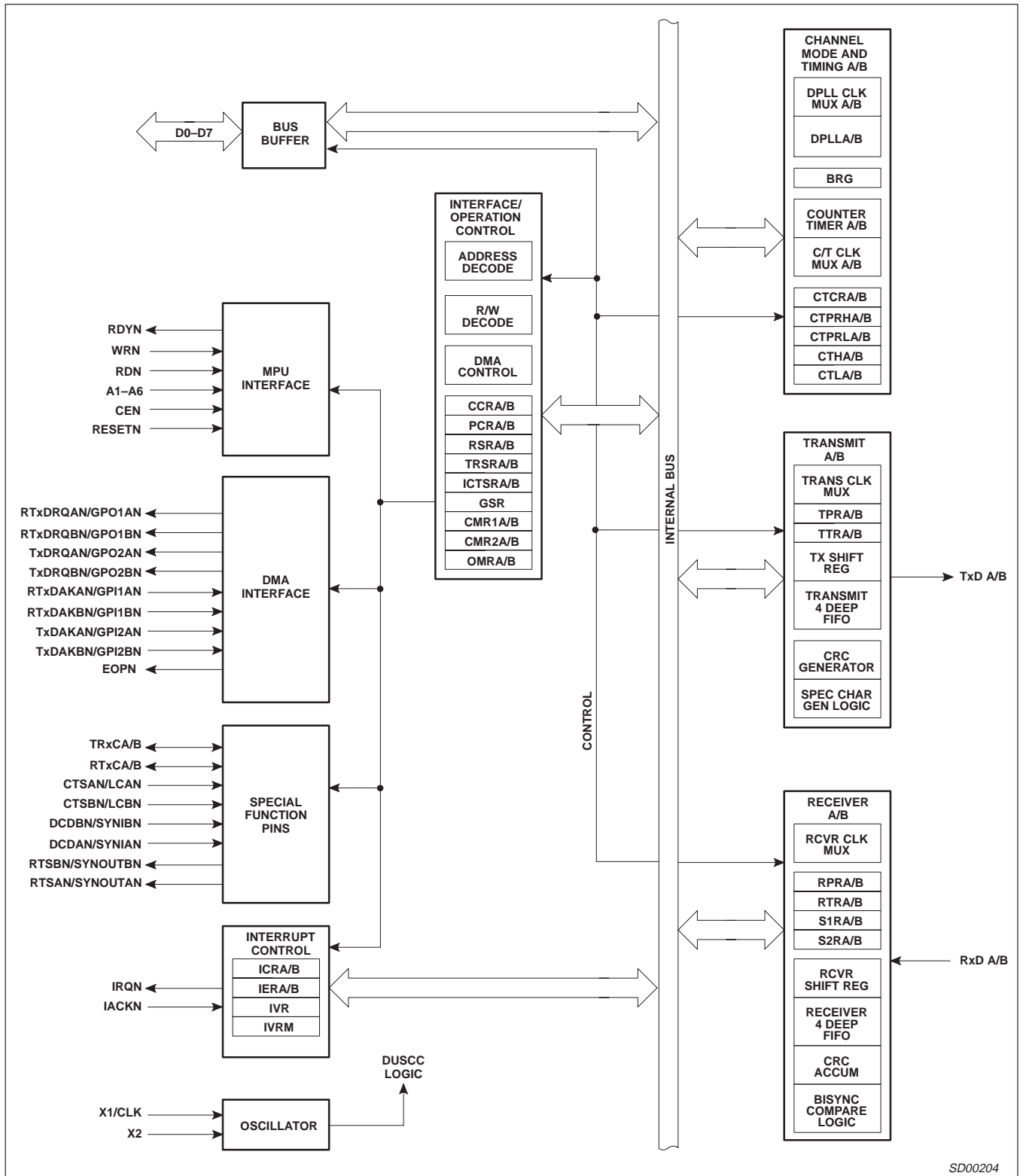


Figure 2. Block Diagram

SD00204

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PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4–2, 47–45	4–2, 51–49	I	Address lines.
D0–D7	31–28, 21–18	33–30, 23–20	I/O	Bidirectional data bus.
RDN	22	24	I	Read strobe.
WRN	26	28	I	Write strobe.
CEN	25	27	I	Chip select.
RDYN	7	8	O	Ready.
IRQN	6	6	O	Interrupt request.
IACKN	1	1	I	Interrupt acknowledge.
X1/CLK	43	47	I	Crystal 1 or external clock.
X2	42	46	I	Crystal 2.
RESETN	23	25	I	Master reset.
RxDA, RxDB	37, 12	40, 14	I	Channel A (B) receiver serial data.
TxDA, TxDB	36, 13	39, 15	O	Channel A (B) transmitter serial data.
RTxCA, RTxCB	39, 10	43, 11	I/O	Channel A (B) receiver/transmitter clock.
TRxCA, TRxCB	40, 9	44, 10	I/O	Channel A (B) transmitter/receiver clock.
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	Channel A (B) clear-to-send input or loop control output.
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	Channel A (B) data carrier detected or external sync.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	Channel A (B) receiver/transmitter DMA service request or general purpose output.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	Channel A (B) transmitter DMA service request, general purpose output or request-to-send.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	Channel A (B) receiver/transmitter DMA acknowledge or general purpose input 1.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	Channel A (B) transmitter DMA acknowledge or general purpose input 2.
EOPN	27	29	I/O	DMA transfer complete.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	Channel A (B) request-to-send or Sync detect.
VCC	48	52	I	Power input.
GND	24	26	I	Signal and power ground.

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DC ELECTRICAL CHARACTERISTICS^{1, 3} $T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage: All except X1/CLK				0.8	V
	X1/CLK				0.4	V
V_{IH}	Input high voltage: All except X1/CLK		2.0			V
	X1/CLK		2.4		V_{CC}	V
V_{OL}	Output low voltage: All except IRQN	$I_{OL} = 5.3\text{mA}$				V
V_{OH}	Output high voltage: (Except open drain outputs)	$I_{OL} = 8.8\text{mA}$			0.5	V
		$I_{OH} = -400\mu\text{A}$	2.4		0.5	V
I_{ILX1}	X1/CLK input low current ³	$V_{IN} = 0$, X2 = GND	-5.5		0.0	mA
I_{IHX1}	X1/CLK input high current ³	$V_{IN} = V_{CC}$, X2 = GND			1.0	mA
I_{ILX2}	X2 input low current ³	$V_{IN} = 0$, X1 = open	-100			μA
I_{IHX2}	X2 input high current ³	$V_{IN} = V_{CC}$, X1 = open			100	μA
I_{IL}	Input low current RESETN, TxDAKN, RxDAKN	$V_{IN} = 0$	-40			μA
I_I	Input leakage current	$V_{IN} = 0$ to V_{CC}	-5		5	μA
I_{OZH}	Output off current high, 3-State data bus	$V_{IN} = V_{CC}$			5	μA
I_{OZL}	Output off current low, 3-State data bus	$V_{IN} = 0$	-5			μA
I_{ODL}	Open drain output low current in off state: EOPN	$V_{IN} = 0$			-25	μA
I_{ODH}	Open drain output high current in off state: IRQN, RDYN		-120			μA
	EOPN, IRQN, RDYN	$V_{IN} = V_{CC}$	-5		5	μA
I_{CC}	Power supply current	$V_O = 0$ to V_{CC}			275	mA
C_{IN}	Input capacitance ²	$V_{CC} = \text{GND} = 0$			10	pF
C_{OUT}	Output capacitance ²	$V_{CC} = \text{GND} = 0$			15	pF
$C_{I/O}$	Input/output capacitance ²	$V_{CC} = \text{GND} = 0$			20	pF

NOTES:

- Parameters are valid over specified temperature range.
- These values were not explicitly tested; they are guaranteed by design and characterization data.
- X1/CLK and X2 are not tested with a crystal installed.

AC ELECTRICAL CHARACTERISTICS^{1, 2, 3, 4} $T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RELREH}	RESETN low to RESETN high	1.2		1.2		μs

NOTES:

- Parameters are valid over specified temperature range.
- All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.8V and 2.0V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 2.4V. All time measurements are referenced at input voltages of 0.4V and 2.4V and output voltages of 1.2V and 2.0V, as appropriate.
- See Figure 17 for test conditions for outputs.
- Tests for open drain outputs are intended to guarantee switching of the output transistor. Measurement of this response is referenced from midpoint of the switching signal to a point 0.2V above the actual output signal level. This point represents noise margin that assures true switching has occurred.

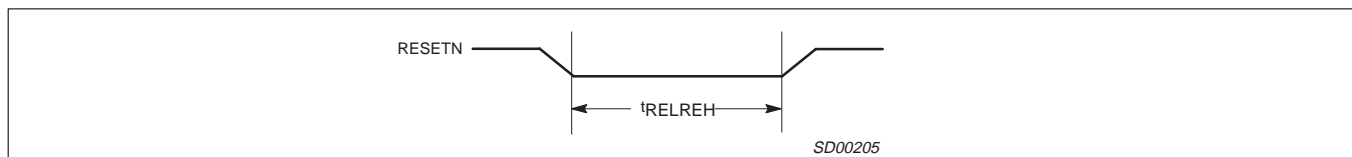


Figure 3. Reset Timing

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AC ELECTRICAL CHARACTERISTICS (Continued)

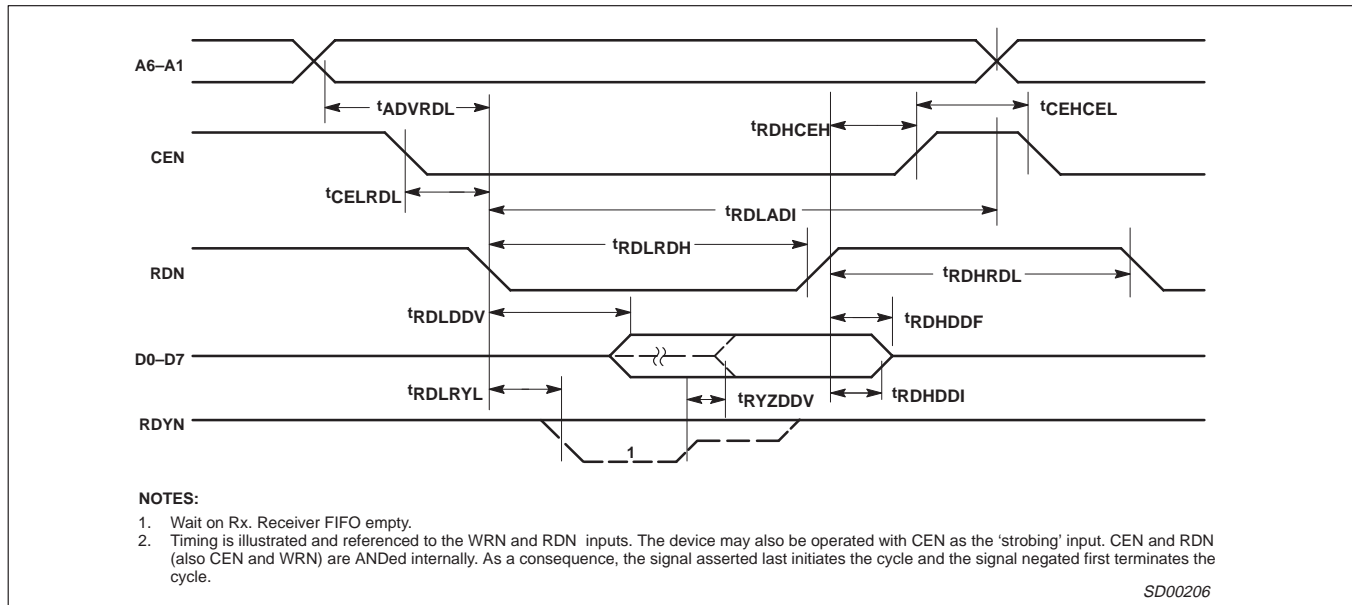


Figure 4. Read Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
tADVRDL	Address valid to RDN low	10		10		ns
tCELRDL	CEN low to RDN low	0		0		ns
tRDLADI	RDN low to address invalid	150		150		ns
tRDLRYL	RDN low to RDYN low		275		275	ns
tRDLLDV	RDN low to read data valid		280		300	ns
tRDLRDH	RDN low to RDN high	300		310		ns
tRYZDDV	RDYN high impedance to read data valid		100		100	ns
tRDHCEH	RDN high to CEN high	0		0		ns
tCEHCEL	CEN high to CEN low	160		170		ns
tRDHDDI	RDN high to read data invalid	10		10		ns
tRDHRDL	RDN high to RDN low	160		170		ns
tRDHDDF	RDN high to data bus floating		75		75	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

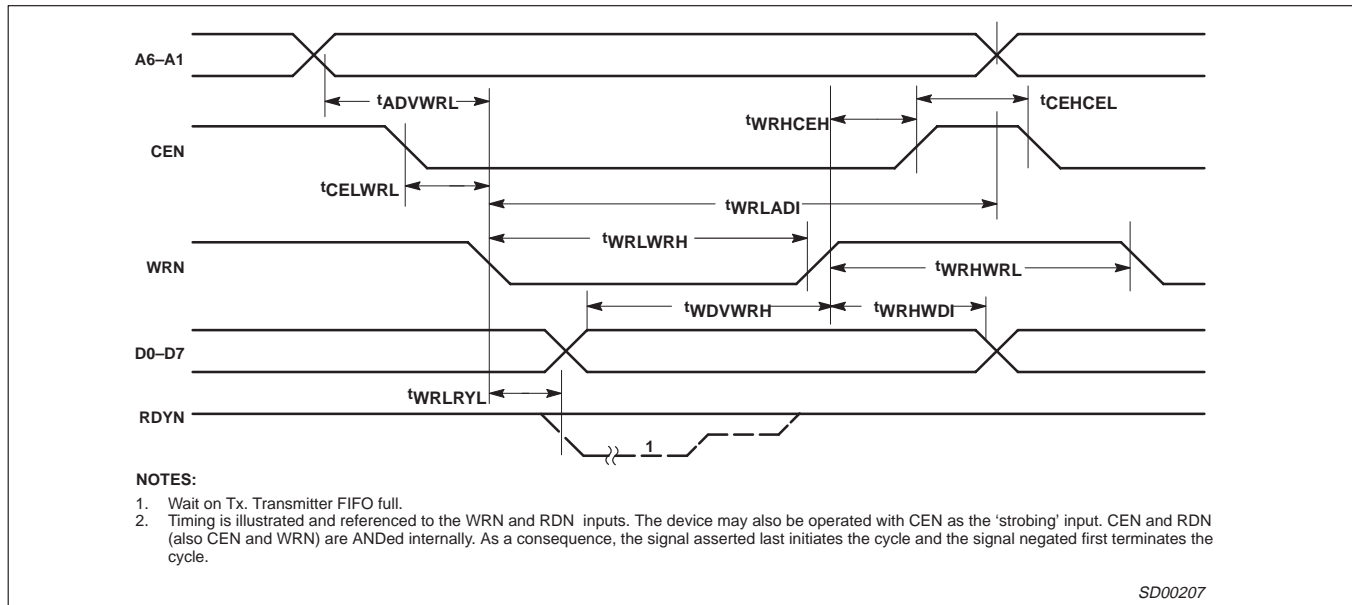


Figure 5. Write Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{ADVWRL}	Address valid to WRN low	10		10		ns
t_{CELWRL}	CEN low to WRN low	0		0		ns
t_{WRLRYL}	WRN low to READY low					ns
t_{WRHCEH}	WRN high to CEN high	0		0		ns
t_{WRLWRH}	WRN low to WRN high	300		310		ns
t_{WDVWRH}	Write data valid to WRN high	100		100		ns
t_{CEHCEL}	CEN high to CEN low	160	275	170	275	ns
t_{WRLADI}	WRN low to address invalid	150		150		ns
t_{WRHWRL}	WRN high to WRN low	160		170		ns
t_{WRHWDI}	WRN high to write data invalid	10		10		ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

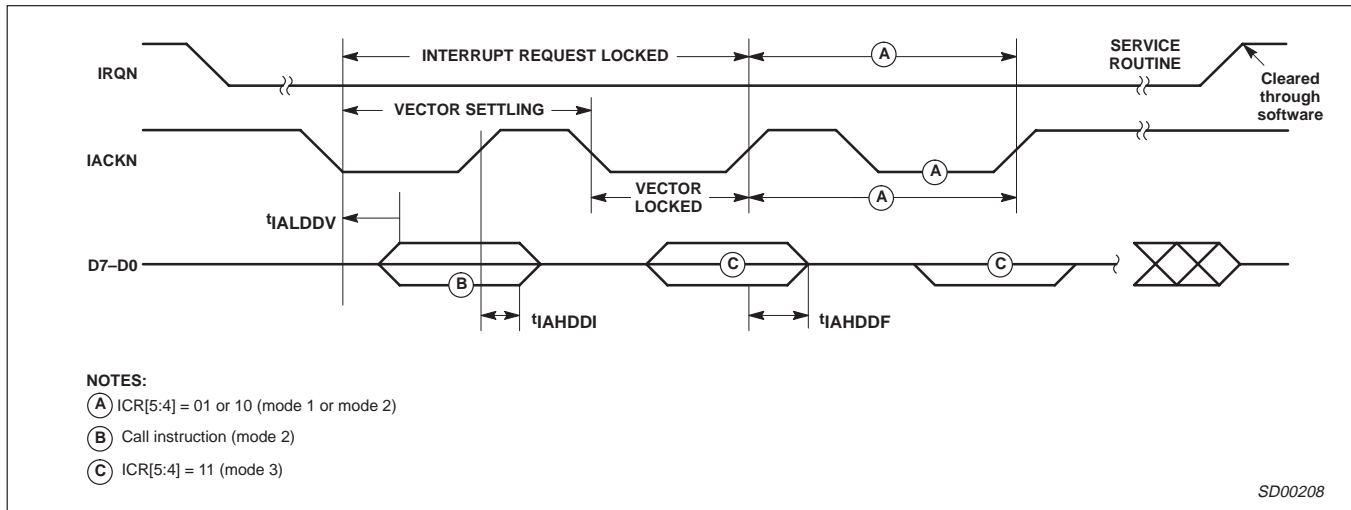


Figure 6. Interrupt Acknowledge Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
tIALDDV	IACKN low to data bus valid		280		280	ns
tIAHDDF	IACKN high to data bus floating		150		150	ns
tIAHDDI	IACKN high to data bus invalid	10		10		ns

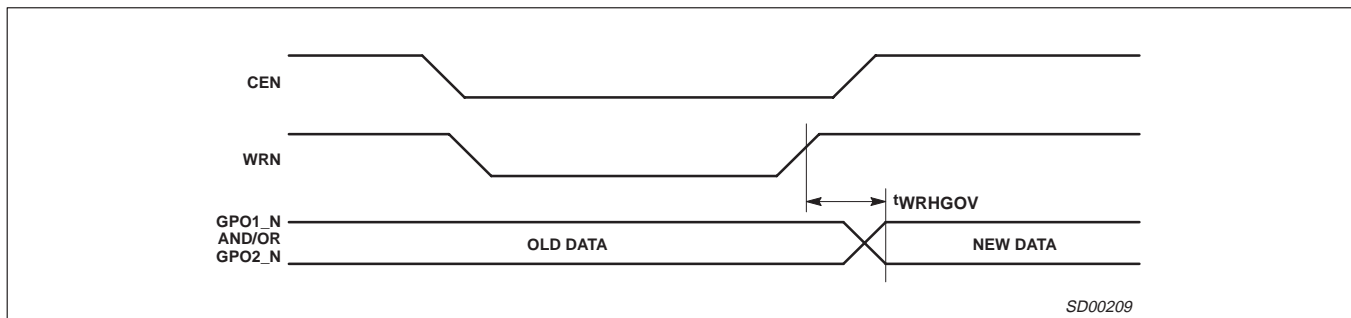


Figure 7. Output Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
tWRHGOV	WRN high to GPO output data valid		300		300	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

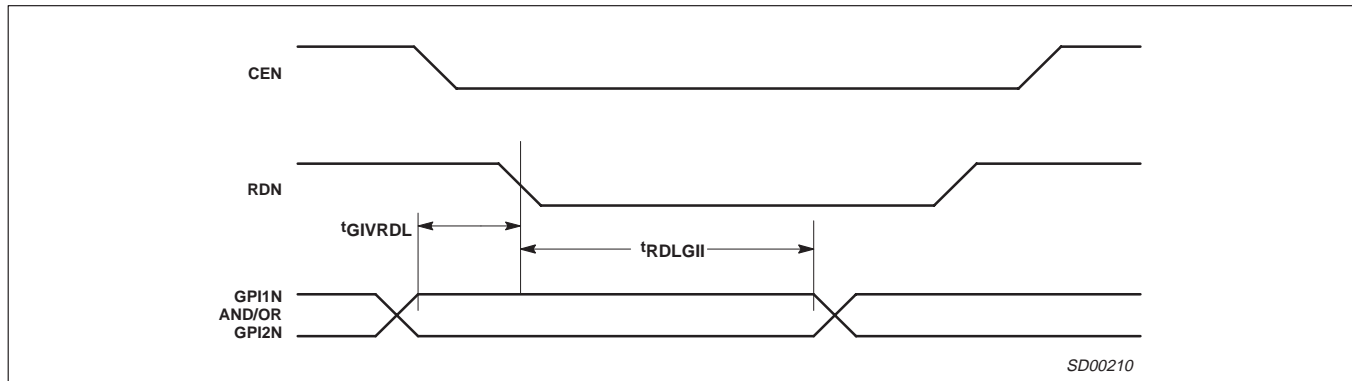


Figure 8. Input Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{GIVRDL}	GPI input valid to RDN low	20		20		ns
t_{RDLGII}	RDN low to GPI input invalid	100		100		ns

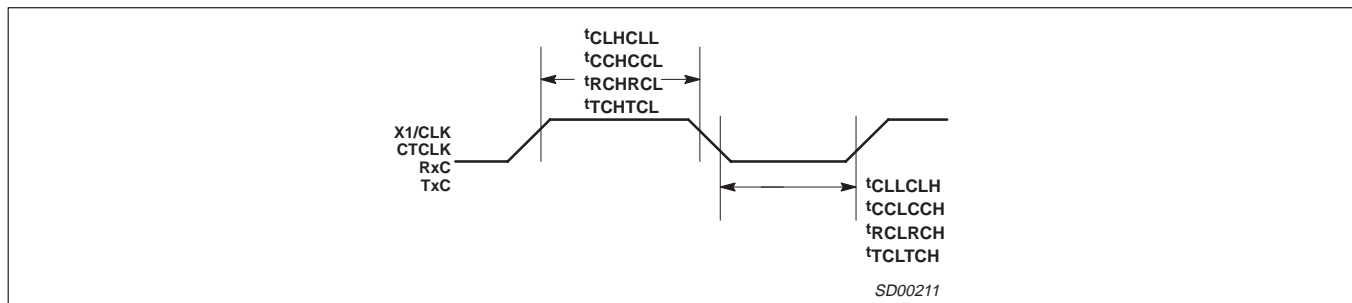


Figure 9. Clock

SYMBOL	PARAMETER	LIMITS						UNIT
		SCN26562C4			SCN26562C2			
		Min	Typ	Max	Min	Typ	Max	
t_{CLHCLL}	X1/CLK high to low time	25			25			ns
t_{CLLCLH}	X1/CLK low to high time	25			25			ns
t_{CCHCCL}	C/T CLK high to low time	100			100			ns
t_{CCLCCH}	C/T CLK low to high time	100			100			ns
t_{RCHRCL}	RxC high to low time	110			150			ns
t_{RCLRCH}	RxC low to high time	110			150			ns
t_{TCHTCL}	TxC high to low time	110			150			ns
t_{TCLTCH}	TxC low to high time	110			150			ns
f_{CL}	X1/CLK frequency	2.0	14.7456	16.0	2.0	14.7456	16.0	MHz
f_{CC}	C/T CLK frequency	0		4.0	0		4.0	MHz
f_{RC}	RxC frequency (16X or 1X)	0		4.0	0		2.5	MHz
f_{TC}	TxC frequency (16X or 1X)	0		4.0	0		2.5	MHz

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AC ELECTRICAL CHARACTERISTICS (Continued)

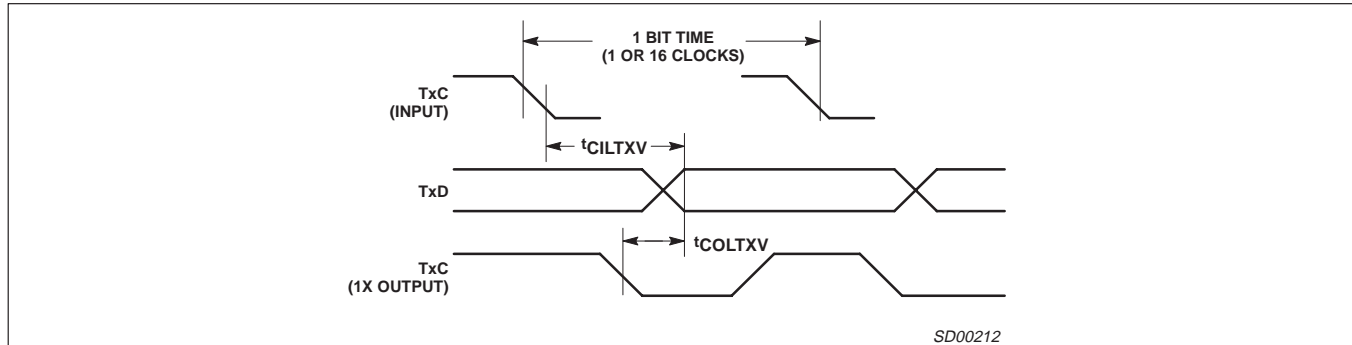


Figure 10. Transmit Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{CILTXV}	TxC input low (1X) to TxD output TxC input low (16X) to TxD output		240 435		240 435	ns
t_{COLTXV}	TxC output low to TxD output		50		50	ns

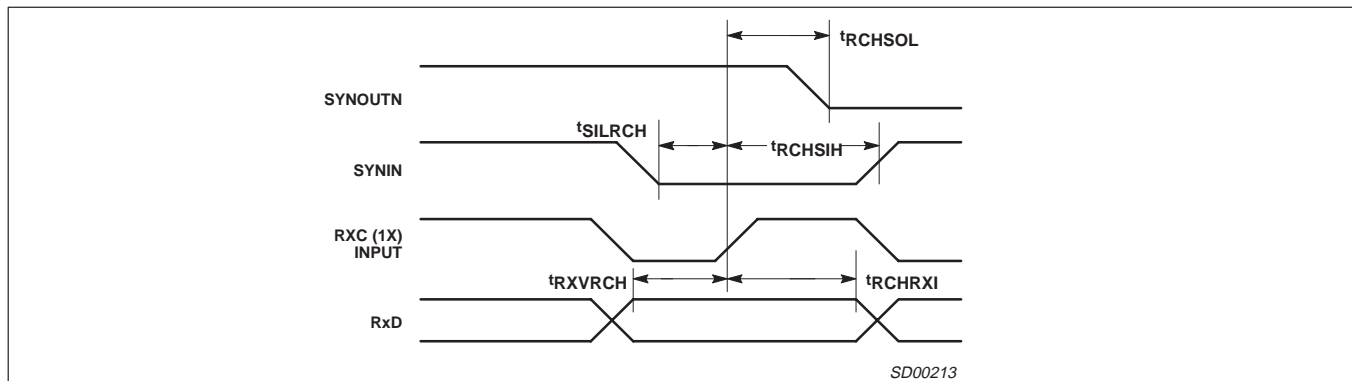


Figure 11. Receive Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RXVRCH}	RxD data valid to RxC high: For NRZ data For NRZI, Manchester, FM0, FM1 data	50 120		50 130		ns ns
t_{RCHRXI}	RxC high to RxD data invalid: For NRZ data For NRZI, Manchester, FM0, FM1 data	50 10		50 10		ns ns
t_{SILRCH}	SYNIN low to RxC high	100		100		ns
t_{RCHSIH}	RxC high to SYNIN high	50		50		ns
t_{RCHSOL}	RxC high to SYNOUTN low		300		300	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

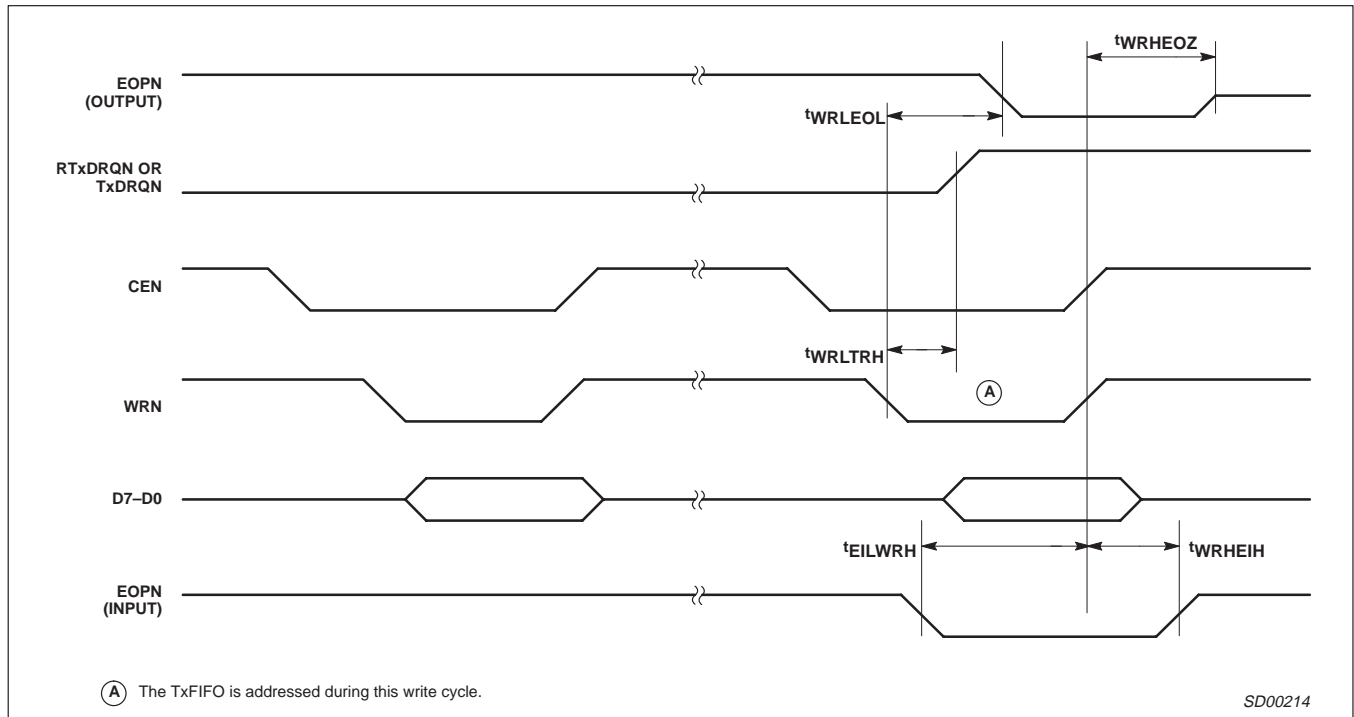


Figure 12. Transmit Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
tWRLTRH	WRN low to Tx DMA REQ high		320		320	ns
tWRLEOL	WRN low to EOPN output low		225		225	ns
tWRHEOZ	WRN high to EOPN output high impedance		225		225	ns
tEILWRH	EOPN input low to WRN high	50	225	50	225	ns
tWRHEIH	WRN high to EOPN input high	50		50		ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

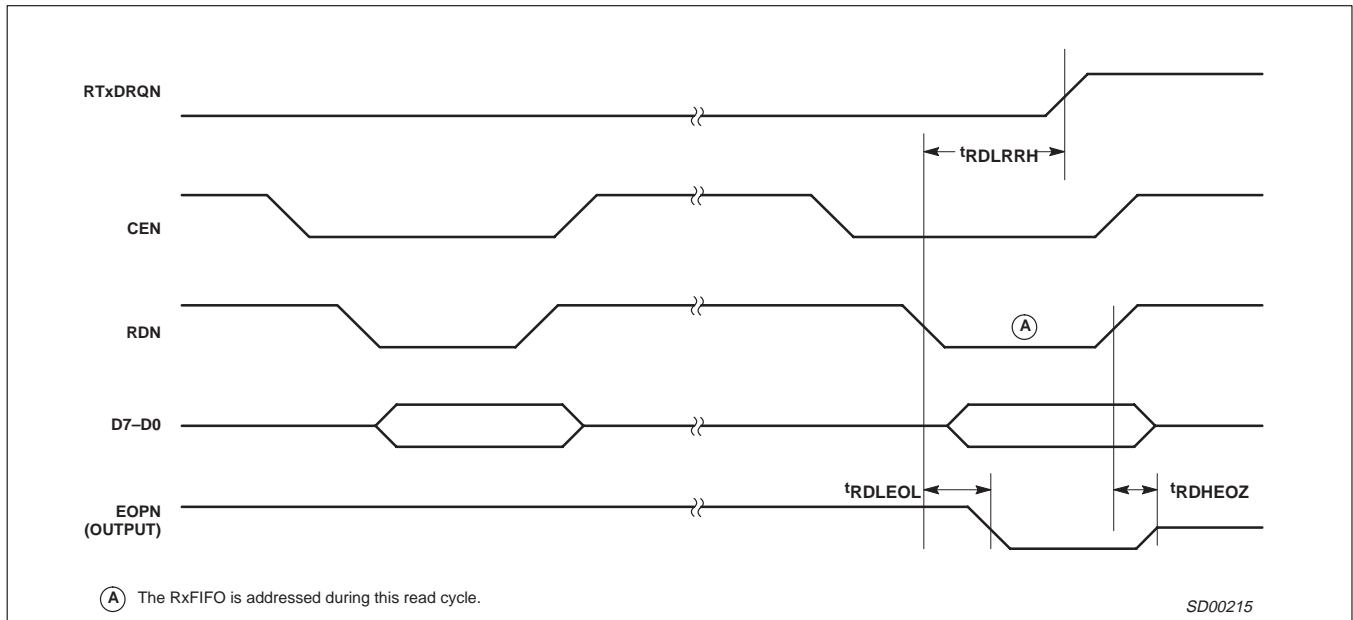


Figure 13. Receive Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
tRDLRRH	RDN low to Rx DMA REQn high		320		320	ns
tRDLEOL	RDN low to EOPN output low		300		300	ns
tRDHEOZ	RDN high to EOPN output high impedance		225		225	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

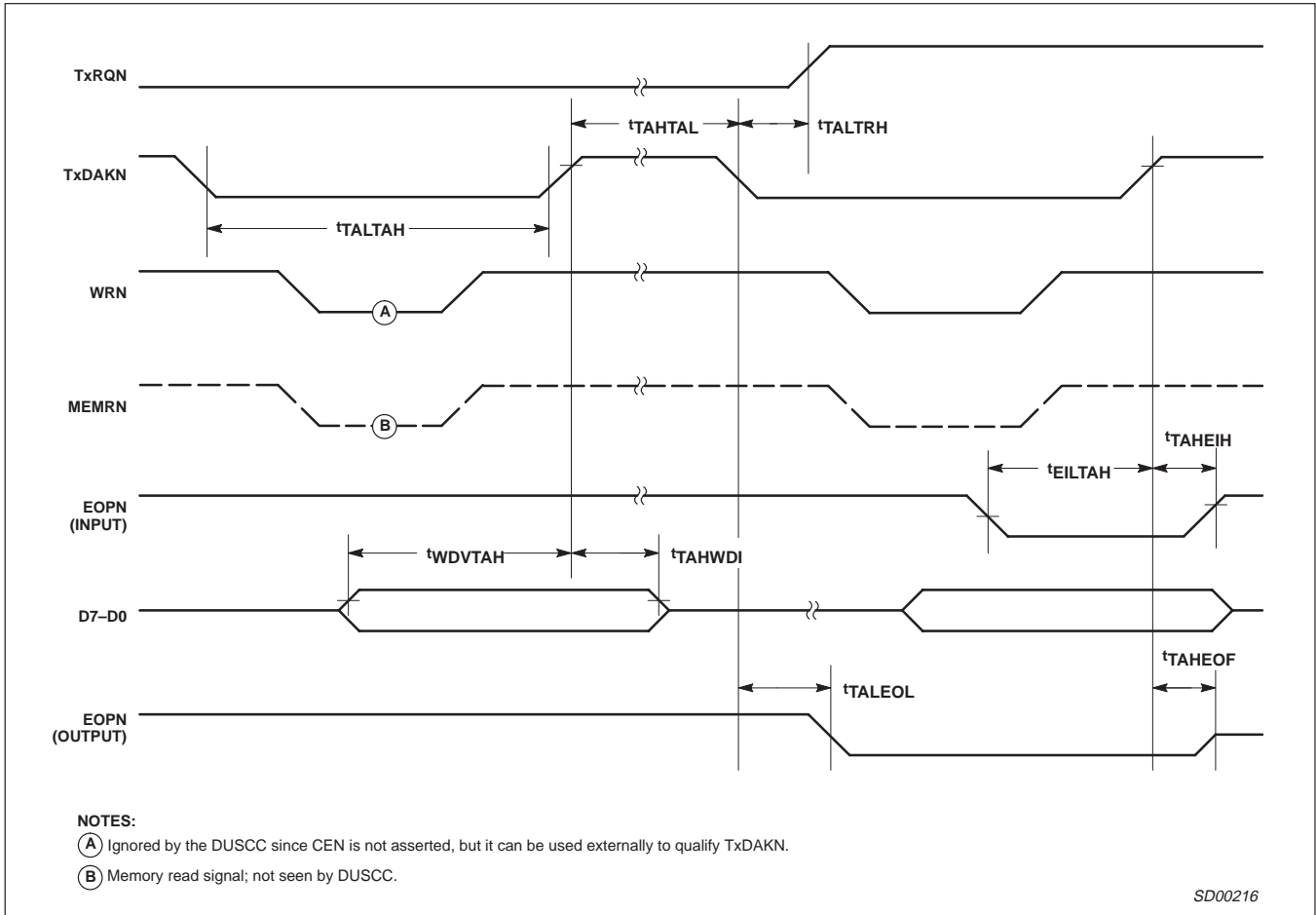


Figure 14. DMA-Transmit Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
tTAHTAL	Transmit DMA ACKN high to low time	100		100		ns
tTALTAH	Transmit DMA ACKN low to high time	250		250		ns
tTALTRAH	Tx DMA ACKN low to Tx DMA REQN high					ns
tWDVTAH	Write data valid to Tx DMA ACKN high	90	250	90	250	ns
tTAHWDI	Tx DMA ACKN high to write data invalid	30		30		ns
tTALEOL	Tx DMA ACKN low to EOPN output low					ns
tTAHEOF	Tx DMA ACKN high to EOPN output float		170		170	ns
tEILTAH	EOPN input low to Tx DMA ACKN high	50	200	50	200	ns
tTAHEIH	Tx DMA ACKN high to EOPN input high	50		50		ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

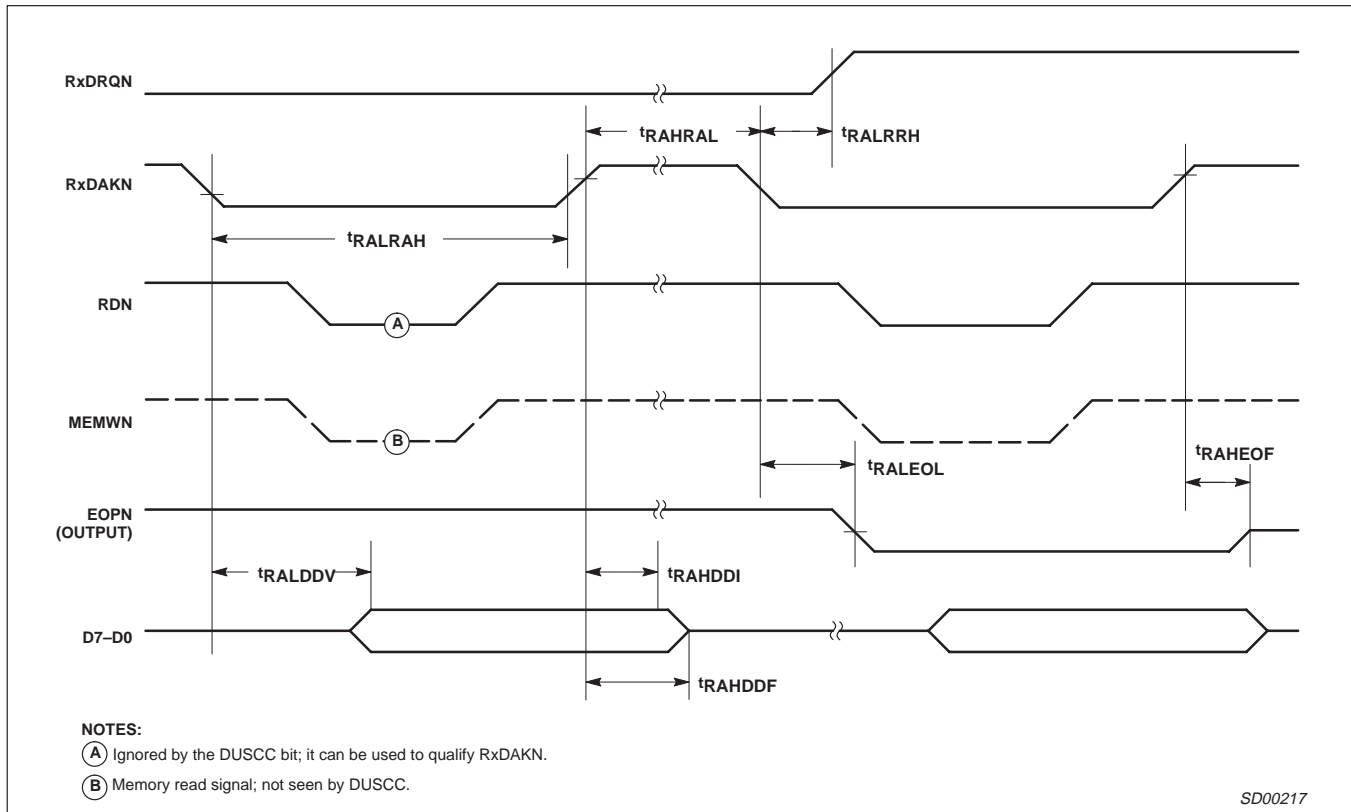


Figure 15. DMA-Receive Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RAHRAL}	Receive DMA ACKN high to low time	160		160		ns
t_{RALRAH}	Receive DMA ACKN low to high time	250		250		ns
t_{RALRRH}	Rx DMA ACKN low to Rx DMA REQ high		320		320	ns
t_{RALEOL}	Rx DMA ACKN low to EOPN output low		200		200	ns
t_{RAHEOF}	Rx DMA ACKN high to EOPN output float		225		225	ns
t_{RALDDV}	Rx DMA ACKN low to read data valid		225		225	ns
t_{RAHDDI}	Rx DMA ACKN high to read data invalid	10		10		ns
t_{RAHDDF}	Rx DMA ACKN high to data bus float		125		125	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

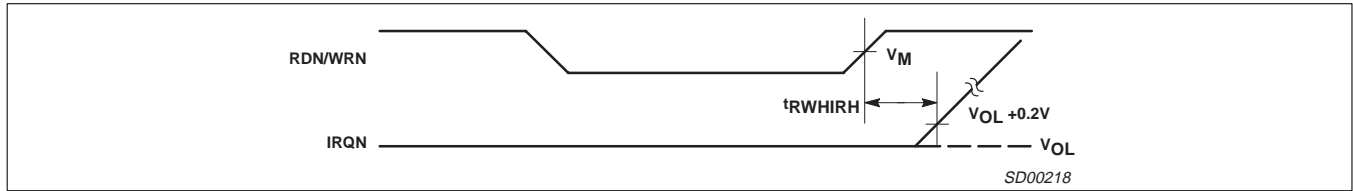


Figure 16. Interrupt Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t _{RWHIRH}	RDN/WRN high to IRQN high for:					
	Read Rx FIFO (RxRDY interrupt)		450		450	ns
	Write Tx FIFO (TxRDY interrupt)		450		450	ns
	Write RSR (Rx condition interrupt)		400		400	ns
	Write TRSR (Rx/Tx interrupt)		400		400	ns
	Write ICTSR (counter/timer interrupt)		400		400	ns

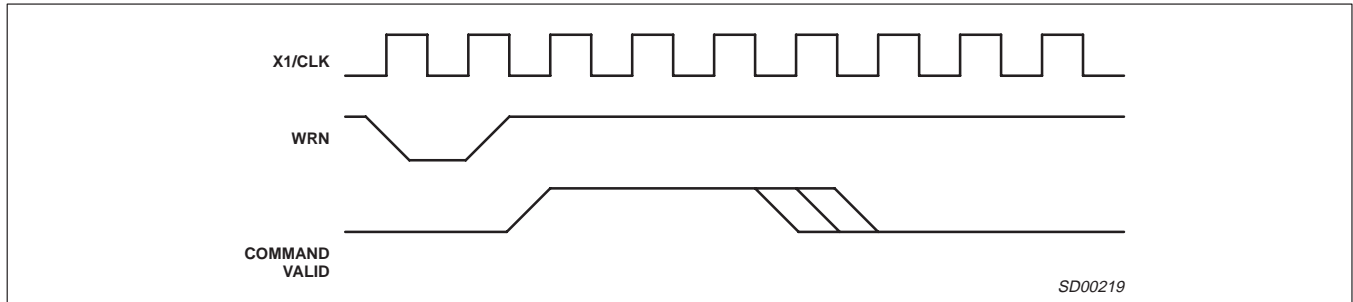


Figure 17. Command Timing

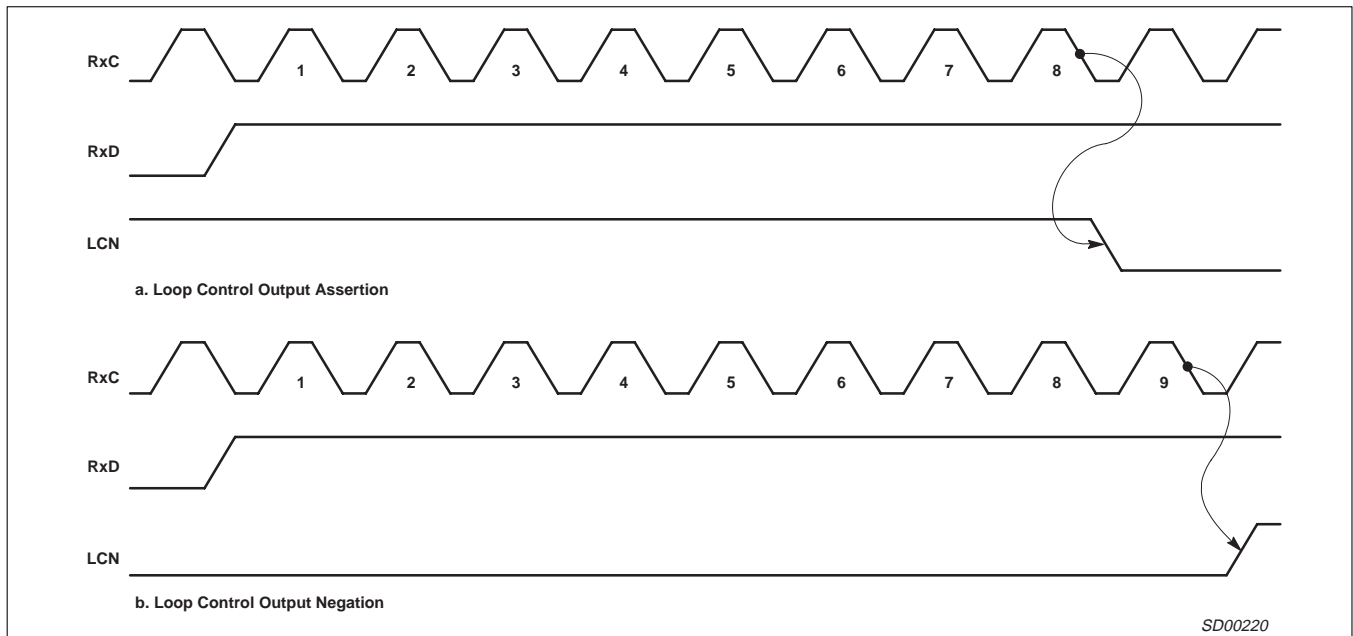


Figure 18. Relationship Between Received Data and the Loop Control Output

Dual universal serial communications controller (DUSCC)

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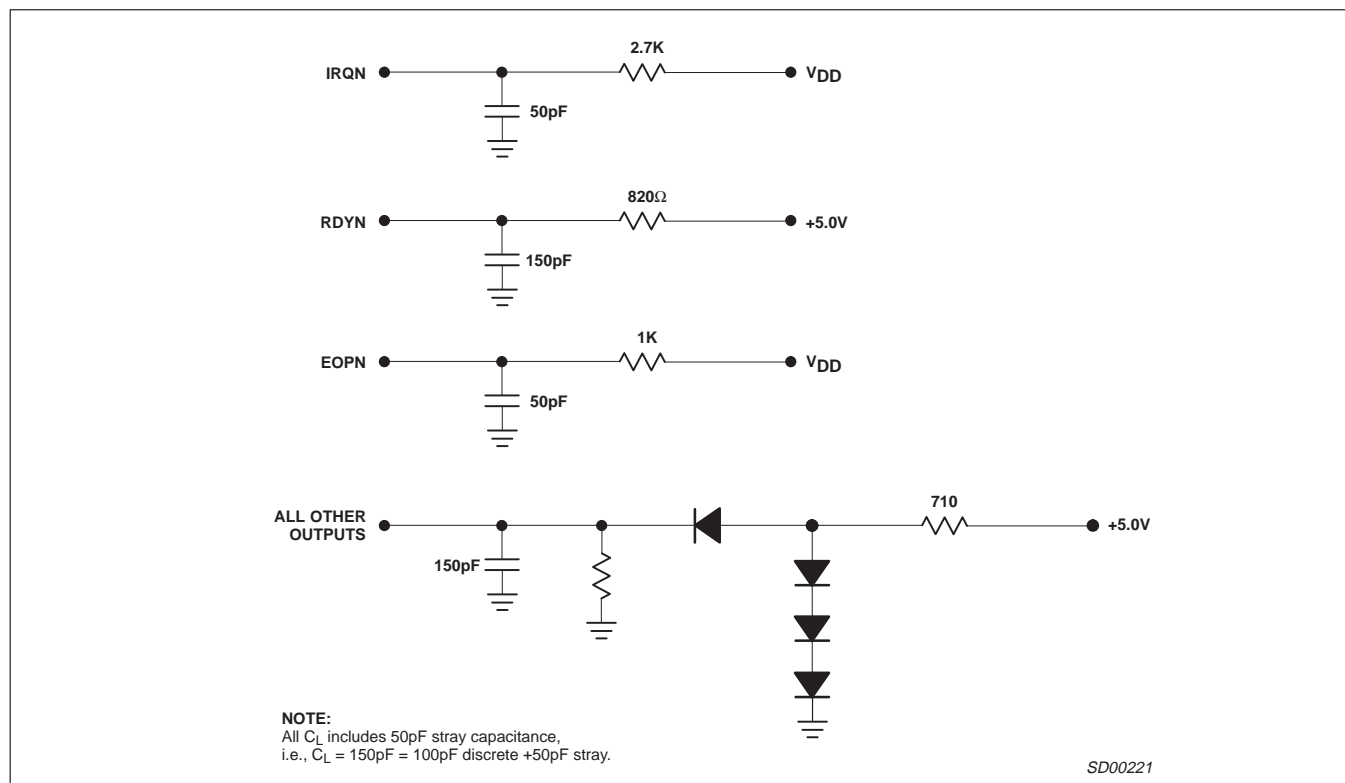


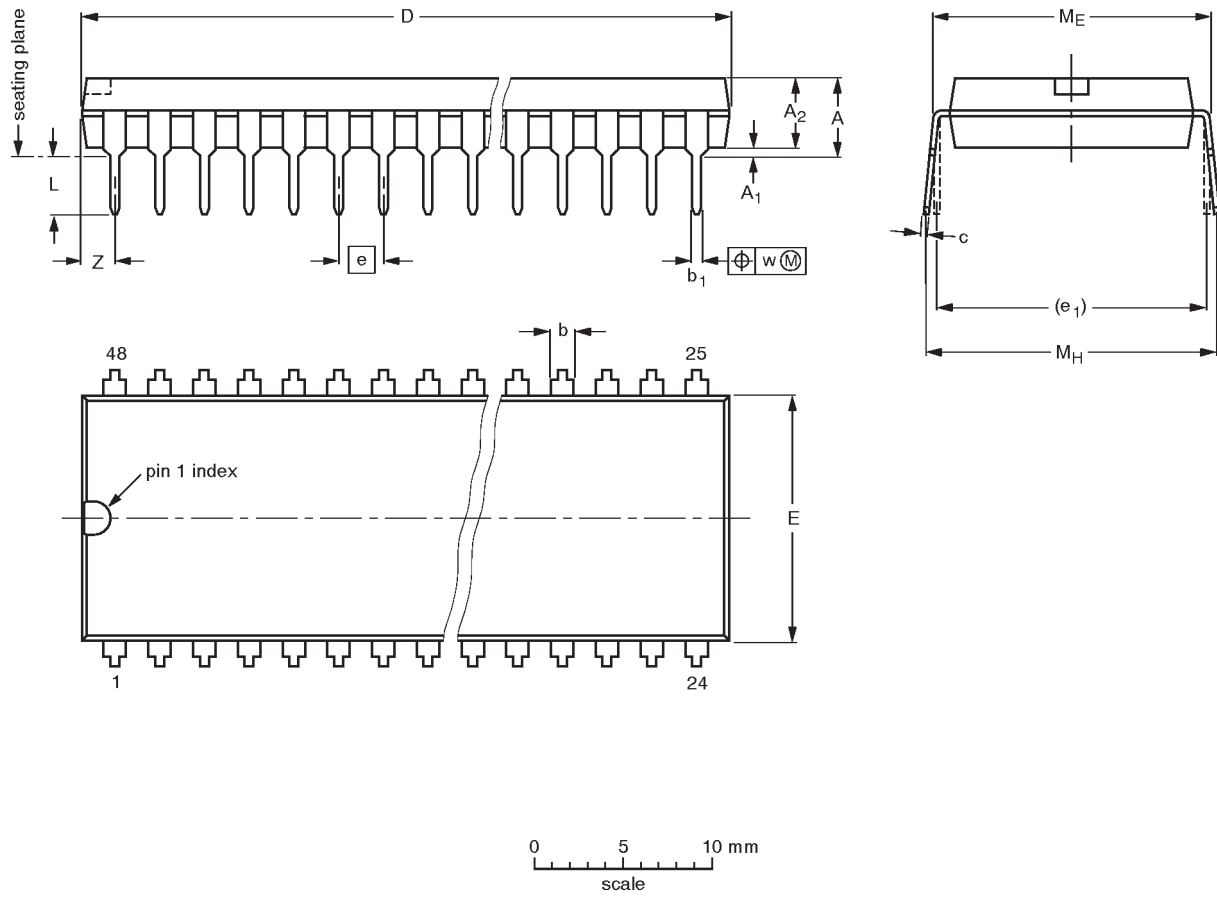
Figure 19. Test Conditions for Outputs

Dual universal serial communications controller (DUSCC)

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DIP48: plastic dual in-line package; 48 leads (600 mil)

SOT240-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.9	0.36	4.06	1.4 1.14	0.53 0.38	0.36 0.23	62.60 61.60	14.22 13.56	2.54	15.24	3.90 3.05	15.88 15.24	18.46 15.24	0.254	2.1
inches	0.19	0.014	0.16	0.055 0.045	0.021 0.015	0.014 0.009	2.46 2.42	0.56 0.53	0.10	0.60	0.15 0.12	0.63 0.60	0.73 0.60	0.01	0.083

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

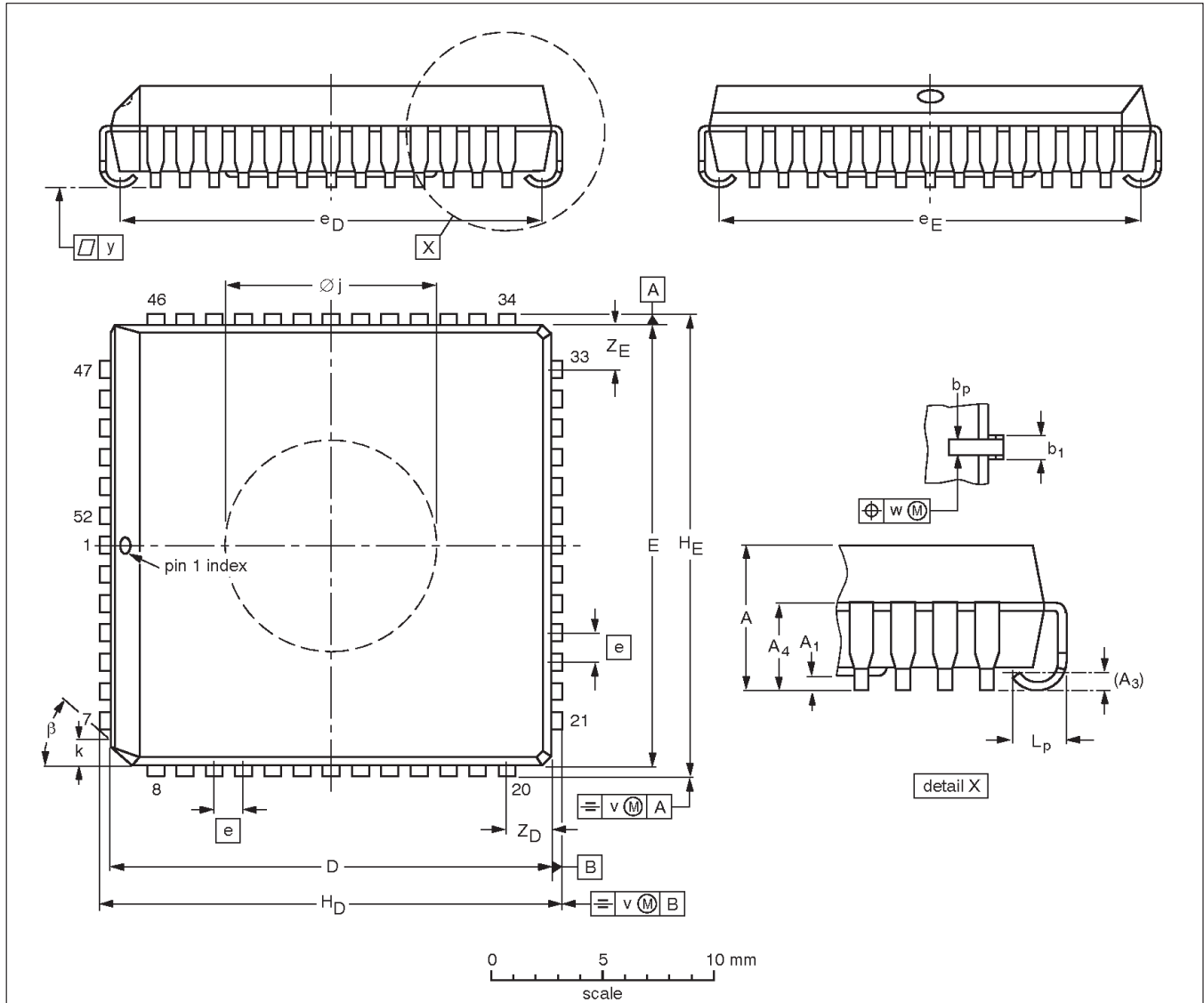
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT240-1						92-11-17 95-01-25

Dual universal serial communications controller (DUSCC)

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PLCC52: plastic leaded chip carrier; 52 leads; pedestal

SOT238-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A ₁ min.	A ₃	A ₄ max.	b _p	b ₁	D ⁽¹⁾	E ⁽¹⁾	e	e _D	e _E	H _D	H _E	k	∅ _j	L _p	v	w	y	Z _D ⁽¹⁾ max.	Z _E ⁽¹⁾ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	19.20 19.05	19.20 19.05	1.27	18.54 17.53	18.54 17.53	20.19 19.94	20.19 19.94	1.22 1.07	9.25 9.09	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.756 0.750	0.756 0.750	0.05	0.730 0.690	0.730 0.690	0.795 0.785	0.795 0.785	0.048 0.042	0.364 0.358	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT238-3		MO-047AD			95-02-25- 97-12-16

Dual universal serial communications controller (DUSCC)

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NOTES

Dual universal serial communications controller (DUSCC)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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